SCAN BASED DELAY MEASUREMENT TECHNIQUE USING CONFIGURABLE SIGNATURE REGISTER

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ABSTRACT
With the scaling of semiconductor process technology, performance of modern VLSI chips will improve significantly. However, as the scaling increases, small-delay defects which are caused by resistive-short, resistive-open, or resistive-via become serious problems. The proposed method uses a signature analysis and a scan design to detect small delay defects. The proposed measurement technique measures the delay of the explicitly sensitized paths with the resolution of the on-chip variable clock generator. The proposed scan design realizes complete on-chip delay measurement in short measurement time using the proposed delay measurement technique and extra latches for storing the test vectors.

KEY WORDS: Very Large Scale Integration, Design for testability, Signature register, Large Scale Integration, Delay Estimation.

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REFERENCES


