DESIGN OF HIGH SPEED AND LOW POWER ALU VEDIC MATHEMATICS

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ABSTRACT
This paper is devoted for designing high speed arithmetic logic unit. All of us know that ALU is a module which can perform arithmetic and logic operations. The reason behind choosing this topic as a research work is that, ALU is the key element of digital processors like as microprocessors, microcontrollers, central processing unit etc. Every digital domain based technology depends upon the operations performed by ALU either partially or whole. That’s why it highly required designing high speed ALU, which can enhance the efficiency of those modules which lies upon the operations performed by ALU. The speed of ALU greatly depends upon the speed of multiplier. There are so many multiplication algorithms exist now-a-days at algorithmic and structural level. Our work proved that Vedic multiplication technique is the best algorithm in terms of speed. Further we have seen that the conventional Vedic multiplication hard wares have some limitations. So to overcome those limitations a novel approach has been proposed to design the Vedic multiplier with the use of unique addition tree structure, which is used to add partially generated products. For designing the two bit Vedic multiplier conventional hardware of Vedic multiplier has been used. For designing the four and eight bit level Vedic multiplier divide and conquer approach has been used. After designing the proposed Vedic multiplier, it has been integrated into an eight bit module of arithmetic logic unit along with the conventional adder, subtractor.. All of these operational sub-modules (adder, subtractor, multiplier) have been designed as the combinatorial circuit. And for the synchronization of these operational sub-modules, the multiplexers which have been used to integrate these sub-modules in a single unit have been triggered by positive edge

KEY WORDS: Vedic Urdhva Triyambakam multiplication algorithm, Arithmetic Unit, Arithmetic Logic Unit, Addition tree structure.

References


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