DESIGN AND SIMULATION OF APPROXIMATE ADDERS FOR LOW POWER DIGITAL SIGNAL PROCESSING APPLICATIONS

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ABSTRACT

Low power is the imperative requirement for portable multimedia devices employing several signal processing algorithms and architectures. Earlier research exploits error resiliency primarily through voltage over scaling, using algorithmic and architectural techniques to mitigate the resulting errors. In our paper, we propose logic complexity reduction at the transistor level as the alternative approach to take advantage of the relaxation of numerical accuracy. We examined this concept by proposing several imprecise or approximate full adder cell with reduced complexity at the transistor level, and used them to design approximate multi-bit adders. In addition to an inherent reduction in switched capacitance, our tier result in significantly shorter critical paths, enabling voltage scaling. We implement our concept in the application of Noise Cancellation algorithms (LMS algorithm). Simulation outputs indicate up to 69% power savings using the proposed approximate adders, when compared to previous implementations using accurate adders.

KEY WORDS: Approximate computing, less power, mirror adder.

REFERENCES


